IPC J-STD-001ES
December 2010

JOINT INDUSTRY STANDARD

Space Applications Electronic Hardware Addendum to IPC J-STD-001E Requirements for Soldered Electrical and Electronic Assemblies

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IPC J-STD-001ES

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Developed by the Space Electronic Assemblies J-STD-001 Addendum Task Group (5-22as) of the Assembly & Joining Processes Committee (5-20) of IPC

Users of this publication are encouraged to participate in the development of future revisions.

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Acknowledgment

Members of the Space Electronic Assemblies J-STD-001 Addendum Task Group have worked together to develop this document. We would like to thank them for their dedication to this effort. Any document involving a complex technology draws material from a vast number of sources. While the principal members of the Space Electronic Assemblies J-STD-001 Addendum Task Group (5-22as) of the Assembly & Joining Processes Committee (5-20) are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

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The following topics are addressed in this Addendum.

The following reference numbers are to J-STD-001E Clauses that are modified or added in this addendum.

Space Applications Electronic Hardware Addendum to IPC J-STD-001E Requirements for Soldered Electrical and Electronic Assemblies

0.1 Scope This Addendum provides requirements to be used in addition to, and in some cases, in place of, those published in IPC J-STD-001E to ensure the reliability of soldered electrical and electronic assemblies that must survive the vibration and thermal cyclic environments getting to and operating in space.

0.1.1 Purpose When required by procurement documentation/drawings, this Addendum supplements or replaces specifically identified requirements of IPC J-STD-001, Revision E of April 2010.

0.1.2 Precedence The contract takes precedence over this Addendum, referenced standards and User-approved drawings (see IPC J-STD-001E 1.7.1). In the event of a conflict between this Addendum and the applicable documents cited herein, this Addendum takes precedence. Where referenced criteria of this Addendum differ from the published IPC J-STD-001E, this Addendum takes precedence. See Table 1 of this addendum, clauses 1.7 Order of Precedence and 1.7.1 Conflict.

0.1.3 Existing or Previously Approved Designs This Addendum **shall not** constitute the sole cause for the redesign of previously approved designs. When drawings for existing or previously approved designs undergo revision, they should be reviewed and changes made that allow for compliance with the requirements of this Addendum.

0.1.4 Use This Addendum is not to be used as a stand-alone document.

Where criteria are not supplemented, the Class 3 requirements of IPC J-STD-001E **shall** apply. Where IPC J-STD-001E criteria are supplemented or new criteria are added by this Addendum, the clause is listed in J-STD-001ES, Table 1, Space Applications Requirements, and the entire IPC J-STD-001E clause is replaced by this Addendum except as specifically noted.

The clauses modified by this Addendum do not include subordinate clauses unless specifically stated (e.g., 1.4 does not include 1.4.1). Clauses, Tables, Figures, etc. in IPC J-STD-001E that are not listed in this Addendum are to be used as-published.

0.1.5 Lead-Free Tin For the purpose of this document, lead-free tin is defined as tin containing less than 3 percent lead by weight as an alloying constituent. Solder alloy Sn96.3Ag3.7 is exempt from this requirement. See Table 1 of this addendum, clause 3.2.

0.1.6 Use of Lead-Free Tin The use of components, assemblies, packaging technology, mechanical hardware, and materials meeting any of the following conditions **shall** be prohibited unless documented and controlled through a User approved Lead Free Control Plan (LFCP) incorporating either a replating or hot solder dip (HSD) process that completely replaces the lead-free tin finish, or a minimum of two mitigation measures.

- Lead-free Tin platings, metallization, etc., on external surfaces of parts, mechanical parts, etc., or in internal cavity surfaces (i.e.: hybrid, relay crystal cans, MEMS etc)
- Any components, printed circuit assemblies (PCAs), etc. assembled with lead-free tin solder alloys except Sn96.3Ag3.7 (see paragraph 3.2).

0.1.6.1 Lead Free Control Plan The Lead Free Control Plan (LFCP) **shall** document controls and processes that assures that assemblies containing lead-free tin solder alloys and/or component finishes will perform as intended within the expected parameters of the mission, e.g., environment, duration, etc. At a minimum, the LFCP **shall**:

a. Document every incidence of lead-free tin technology and prevent its use without review and approval by the User prior to implementation.
b. Incorporate a minimum of two mitigation measures when the lead-free tin finish is not completely replaced through a replating or HSD process.
c. Include any special design requirements, mitigation measures, test and qualification requirements, quality inspection and screening, marking and identification, maintenance, and repair processes.
d. Require review and approval by the User prior to implementation.

The following documents may be helpful when developing the LFCP:

- GEIA-STD-0005–1, Performance Standard for Aerospace and High Performance Electronic Systems Containing Lead-free Solder

- GEIA-STD-0005–2, Standard for Mitigating the Effects of Tin Whiskers in Aerospace and High Performance Electronic Systems
- GEIA-HB-0005–1, Program Management / Systems Engineering Guidelines For Managing The Transition To Lead-Free Electronics
- GEIA-HB-0005–2, Technical Guidelines for Aerospace and High Performance Electronic Systems Containing Lead-free Solder and Finishes
- GEIA-STD-0006, Requirements for Using Solder Dip to Replace the Finish on Electronic Piece Parts

0.1.6.2 Mitigation Components, sub-assemblies, assemblies, and mechanical hardware identified as having lead-free tin surfaces, platings, metallization, etc., but which by package design or engineering decision are not protected by SnPb replating or HSD, **shall** be protected by at least two process or design mitigation techniques to reduce or eliminate the risks created by metallic whisker formation in the expected end-use application/environment. Use of mitigation methods **shall** require technical review and approval by the User prior to implementation. Mitigation measures that may be used are:

a. Design – Components, sub-assemblies, assemblies, and mechanical hardware identified as having external surfaces, platings, metallization, etc. with a lead-free tin finish **shall** be physically positioned or mechanically isolated to ensure the growth of conductive whiskers does not adversely affect performance or reliability. Direct line-of-sight spacing between electrically uncommon conductive surfaces **shall** be sufficient to ensure whisker growth rates (1mm/yr. nominal) over the life of the mission do not violate minimum electrical clearance requirements.
b. External surfaces, platings, metallization, etc., with a lead-free tin finish **shall** be fully coated with conformal coating with a total cured finish of not less than 100 µm [0.004 in].
c. Embedment/Encapsulation – Embedment or encapsulant material **shall** fully wet and cover all surfaces of parts and areas specified by the approved engineering documentation. Cured material **shall** be compatible with the hardware and mission environment, and **shall not** adversely affect hardware performance or reliability.
d. Other mitigation techniques approved by the User prior to use.

0.1.7 Red Plague (Cuprous/Cupric Oxide Corrosion) Red Plague (cuprous/cupric oxide corrosion) can develop in silver-coated soft or annealed copper conductors (component leads, single and multistranded wires and PCB conductors) when a galvanic cell forms between the copper base metal and the silver coating in the presence of moisture (H_2O) and oxygen (O_2). Once initiated, the sacrificial corrosion of the copper base conductor can continue indefinitely in the presence of oxygen. The color of the corrosion by-product (cuprous oxide crystals) may vary depending on the different levels of oxygen available, but is commonly noted as a red/reddish-brown discoloration on the silver coating surface.

Definitions For the purpose of this document:

Desiccant is defined as a chemically-inert media used to absorb moisture from the air within a sealed container or package to induce or sustain a level of dryness (desiccation).

Dew Point is defined as the temperature at which a volume of air at a given atmospheric pressure reaches saturation and the entrained water vapor precipitates and condenses.

Red Plague (Cu_2O) is defined as the sacrificial corrosion of copper in a galvanic interface comprised of silver and copper, resulting in the formation of red cuprous oxide (Cu_2O). Continued exposure to an oxygen rich environment can then lead to black cupric oxide (CuO). Galvanic corrosion is promoted by the presence of moisture and oxygen at an exposed copper-silver interface (i.e.: conductor end, pinhole, scratch, nick, etc.).

Unit Pack is defined as the standardized unit of desiccant material, which at thermal equilibrium with air at +77°F (+25°C), will adsorb at least 3 gm (~0.1 oz) of water vapor at 20% relative humidity (RH) and at least 6 gm (~0.2 oz) of water vapor at 40%RH.

0.1.7.1 Red Plague Control Plan – Minimum Requirements The use of silver-coated copper conductors shall require the implementation of a User-approved Red Plague Control Plan (RPCP) to reduce and control exposure to environmental conditions and contamination that promote the development of cuprous/cupric oxide corrosion (Red Plague) and latent damage. The minimum requirements are as outlined below:

0.1.7.1.1 Shipping and Storage Wire and cable shall be shipped and stored in sealed water-vapor-proof packaging (i.e.: Moisture Barrier Bag, dry pack, etc.), with capped ends, activated desiccant, and humidity indicator card. Silver-coated copper wire and cable shall be segregated and dispositioned if the humidity indicator card registers 70% or more RH.

a. Water-vapor-proof protection packaging **shall** meet MIL-STD-2073–1E Method 51. Moisture Barrier Bags (MBB) **shall** meet MIL-PRF-81705, TYPE 1.
b. Capping. Wire and cable ends **shall** be capped with heat shrinkable end-caps conforming to SAE-AMS-DTL-23053/4, or sealed with a material such as an insulating electrical varnish for a length of approximately 25 mm (1 in.).

c. Desiccant (Activated). The bagged, activated desiccant **shall** conform to MIL-D-3464 Type 2 or equivalent. The minimum quantity of desiccant to be used (unit packs) **shall** be based on the protective package's interior exposed surface area, in accordance with MIL-STD-2073–1E, Method 50, Formula 1, or equivalent.

d. Humidity Indicator Card. The humidity indicator card shall be either an Irreversible Indication (50-60-70-80-90% RH) card or a combination Irreversible/Reversible Humidity Indicator (50-60-70-80-90% RH) card conforming to MIL-I-8835 or equivalent.

0.1.7.1.2 Assembly All assembly processes, including receiving inspection and kitting, shall be conducted in an environmentally-controlled and monitored area where dew point is not attained and the relative humidity is less than 70% RH.

a. Wire and cable **shall** not be removed from its protective packaging until it has reached thermal equilibrium with the assembly environment to prevent condensation.

b. Aqueous solvents **shall not** be used for cleaning and flux removal.

0.1.7.1.3 Limited Life Article

a. Silver-coated copper conductors that have exceeded a shelf life of 10 years from manufacturing date **shall not** be used on assemblies fabricated to this standard.

b. Completed assemblies incorporating silver-coated copper conductors with a storage or use life exceeding 10 years from date of assembly **shall** be identified, inspected and tested, and tracked as a limited-life article.

J-STD-001ES Table 1 Space Applications Requirements

J001E Reference	Space Applications Requirement (as changed by this Addendum)
1.1	**NOTE:** This clause is unchanged from J-STD-001E. It is included here to clarify that the Scope of the space addendum does not replace nor alter Scope of the base document. **Scope** This standard prescribes practices and requirements for the manufacture of soldered electrical and electronic assemblies. Historically, electronic assembly (soldering) standards contained a more comprehensive tutorial addressing principles and techniques. For a more complete understanding of this document's recommendations and requirements, one may use this document in conjunction with IPC-HDBK-001, IPC-A-610 and IPC-HDBK-610.
1.2	**NOTE:** This clause is unchanged from J-STD-001E. It is included here to clarify that the Purpose of the space addendum does not replace nor alter Purpose of the base document. **Purpose** This standard describes materials, methods and acceptance criteria for producing soldered electrical and electronic assemblies. The intent of this document is to rely on process control methodology to ensure consistent quality levels during the manufacture of products. It is not the intent of this standard to exclude any procedure for component placement or for applying flux and solder used to make the electrical connection.
1.5.1	**Hardware Defects** When the word "**shall**" is used it expresses a requirement that is mandatory. Hardware characteristics or conditions that do not conform to the requirements of this specification that are detectable by inspection or analysis **shall** be classified as hardware defects. Hardware defects **shall** be identified, documented and dispositioned, e.g., rework, scrap, use as is, or repair. It is the responsibility of the User (see 1.8.13) to define additional or unique defect categories applicable to the product. It is the responsibility of the Manufacturer (see 1.8.5) to identify defects that are unique to the assembly process (see 1.13.2).
1.7	**Order of Precedence** The contract takes precedence over this Addendum, J-STD-001E, referenced standards and User-approved drawings (see IPC J-STD-001ES 1.7.1). See clause 0.1.2 of this Addendum.
1.7.1	**Conflict** In the event of conflict between the requirements of this standard and the applicable assembly drawing(s)/documentation, the applicable User approved assembly drawing(s)/documentation govern. In the event of a conflict between the text of this standard and the applicable documents cited herein, the text of this standard takes precedence. In the event of conflict between the requirements of this standard and an assembly drawing(s)/ documentation that has not been User approved, this standard governs. See clause 0.1.2 of this Addendum. The User (customer) has the responsibility to specify acceptance criteria. If no criteria is specified, required, or cited, criteria **shall** be established and agreed upon between the Manufacturer and User. When IPC J-STD-001 is cited or required by contract, the requirements of IPC-A-610 do not apply unless separately or specifically required. When IPC-A-610 or other related documents are cited along with IPC J-STD-001 the order of precedence **shall** be defined in the procurement documents.
1.9	**Requirements Flowdown** When this standard is contractually required, the applicable requirements of this standard **shall** be imposed on all applicable contracts, subcontracts, assembly drawing(s), documentation and purchase orders. Unless otherwise specified the requirements of this standard are not imposed on the manufacture or procurement of commercial-off-the-shelf (COTS or catalog) components, assemblies, subassemblies and/or hardware. When a component part is adequately defined by a specification, then the requirements of this standard should be imposed on the manufacture of that part only when necessary to meet end-item requirements. When it is unclear where flowdown should stop, it is the responsibility of the Manufacturer to establish that determination with the User. When an assembly (i.e. daughterboard) is procured, that assembly should meet the requirements of this standard. If the assembly is manufactured by the same Manufacturer, the solder requirements are as stated in the contract for the entire assembly. When a COTS item is to be integrated into a next-level assembly or sub-assembly by use of soldering processes, the COTS' external solderable interconnect points (e.g., terminals, pins, etc.) **shall** meet the solderability requirements of J-STD-001E Clause 4.3. The design and workmanship of COTS items should be evaluated and modified as required to ensure the end-item meets contract performance requirements. Modifications **shall** meet the applicable requirements of this standard.
1.10	**Personnel Proficiency** All instructors, operators, and inspection personnel **shall** be proficient in the tasks to be performed. Objective evidence of that proficiency **shall** be maintained and be available for review. Objective evidence should include records of training to the applicable job functions being performed, work experience, testing to the requirements of this standard, and/or results of periodic reviews of proficiency. Training **shall** be in accordance with the IPC J-STD-001E Training and Certification Program or User approved training program. All training shall be traceable to a Master IPC Trainer (MIT).

J-STD-001ES Table 1 Space Applications Requirements (cont.)

J001E Reference	Space Applications Requirement (as changed by this Addendum)
1.10.1	**Vision Requirements** (this clause is not in J-STD-001E and is unique to this addendum) The Manufacturer is responsible for ensuring that all instructors, operators and inspection personnel meet vision test requirements as a condition of proficiency. Unless an existing company vision testing program is approved by the User, the following tests **shall** be required. The vision requirements may be met with corrected vision. The vision tests **shall** be administered by a qualified examiner, accepted by the User, using standard instruments and techniques. Results of the visual examinations **shall** be maintained and available for review. The following are minimum vision requirements: a. **Far Vision**. Snellen Chart 20/50. b. **Near Vision**. Jaeger 1 at 355.6 mm (14 inches) or reduced Snellen 20/20, or equivalent. c. **Color Vision**. Ability to distinguish red, green, blue, and yellow colors as prescribed in Dvorine Charts, Ishihara Plates, or AO-HRR Tests.
1.11	**Acceptance Requirements** All products **shall** meet the requirements of the assembly drawing(s)/documentation and the requirements specified herein. Manufacturers **shall** perform 100% inspection using either visual inspection or nondestructive evaluation (NDE). Nondestructive verification techniques **shall** be approved by the User prior to use.
1.13.2.2	**High Frequency Applications** High frequency applications (i.e., radio wave and microwaves) may require part clearances, mounting systems, and assembly designs which vary from the requirements stated herein. When high frequency design requirements prevent compliance with the design and part mounting requirements contained herein, Manufacturers may use alternative designs. Alternative designs, including acceptance criteria **shall** be approved by the User prior to use.
1.13.2.3	**High Voltage Applications** High power applications may require part clearances, mounting systems, and assembly designs which vary from the requirements stated herein. When such design requirements prevent compliance with the design and part mounting requirements contained herein, Manufacturers may use alternative designs. Alternative designs, including acceptance criteria **shall** be approved by the User prior to use.
3.1	**Materials** The materials and processes used to assemble/manufacture electronic assemblies **shall** be selected such that their use, in combination, produce products acceptable to this standard. When major elements of the proven processes are changed (e.g., flux, solder paste, cleaning media or system, solder alloy or soldering system), validation of the acceptability of the change(s) **shall** be performed and documented in accordance with approved tests agreed upon between the Manufacturer and User. The change **shall** be approved by the User prior to use. Major elements may also pertain to a change in bare boards (including supplier), solder resist, or metallization. Limited shelf life items **shall** be stored and controlled in accordance with material manufacturers' recommendations or in accordance with the Manufacturer's documented procedures for controlling shelf life. Limited shelf life items **shall** be traceable by lot number, date code and expiration date.
3.2	**Solder** Solder alloys **shall** be Sn60Pb40, Sn62Pb36Ag2, Sn63Pb37, or Sn96.3Ag3.7 in accordance with J-STD-006 or an equivalent controlled specification. Other solder alloys that provide the service life, performance, and reliability required of the product may be used if all other conditions of this standard are met and objective evidence of such is reviewed and approved by the User prior to use. High temperature solder alloys, e.g., Sn96.3Ag3.7, **shall** only be used where specifically indicated by approved drawings. Flux that is part of flux-cored solder wire or solder paste **shall** meet the requirements of 3.3. Flux percentage is optional.
3.3	**Flux** Flux **shall** be in accordance with J-STD-004 or an equivalent controlled specification. Flux **shall** conform to flux activity levels L0 or L1 of flux materials rosin (RO) or resin (RE). Use of any other flux **shall** be approved by the User prior to use. When other activity levels or flux materials are used, data demonstrating material and process compatibility through testing agreed upon between the Manufacturer and User **shall** be provided. Type H or M fluxes may be used for tinning of solid wires with insulation bonded to the wire, e.g., magnet wire. For all fluxing applications where adequate cleaning is not practical, only flux types RO or RE of the L0 flux activity level, or equivalent, **shall** be used.
3.9	**Soldering Tools and Equipment** Tools and equipment **shall** be selected, used, and maintained such that no damage or degradation that would be detrimental to the designed function of parts or assemblies results from their use. Soldering irons, equipment, and systems **shall** be chosen and employed to provide temperature control and isolation from electrical overstress or ESD (see 4.1), and **shall** be calibrated in accordance with ISO 17025 or ANSI/NCSL-Z540- 1–1994. A tool used to cut leads **shall not** impart shock that damages a component lead seal or internal connection. See Appendix A for guidelines on tool selection and maintenance.

J-STD-001ES Table 1 Space Applications Requirements (cont.)

J001E Reference	Space Applications Requirement (as changed by this Addendum)
4.2.3	**Lighting** Illumination at the surface of workstations **shall** be at least 1000 lm/m2. Light sources should be selected to prevent shadows. **Note:** In selecting a light source, the color temperature of the light is an important consideration. Light ranges from 3000–5000° K enable users to differentiate various metal alloys (i.e. copper leads or Kovar® leads) and contaminants, see 4.18.1.
4.5.1	**Gold Removal** Gold **shall** be removed from at least 95% of the surface to-be-soldered of all component leads, component terminations, and solder terminals. A double tinning process or dynamic solder wave may be used for gold removal prior to mounting the component on the assembly.
4.6	**Thermal Protection** When hand soldering, tinning or reworking a component identified as heat sensitive, protective measures **shall** be taken to minimize component heating or prevent thermal shock, e.g., heat sink, thermal shunt, preheat. If it is not possible to implement an effective heat sink, the component **shall** be preheated. Multilayer Ceramic Chip Capacitors (MLCCs) and "stacked" capacitors containing these parts **shall** be handled as thermal shock sensitive. Heat up and cool down rates **shall** be controlled within the Manufacturers' recommendations. **Note:** Hand soldering with solder irons and tinning operations are particularly at risk. Consult your component manufacturer for heat sensitivity levels, and or hand soldering and pretinning recommendations or guidelines. See 0.1.5 at the beginning of this Addendum for additional requirements on retinning of components.
4.9	**General Part Mounting Requirements** When design restrictions mandate mounting components incapable of withstanding soldering temperatures incident to a particular process, such components **shall** be mounted and soldered to the assembly using a process compatible with the part to be soldered. Parts **shall** be mounted with sufficient clearances between the body and the PCB to assure adequate cleaning and cleanliness testing. Assemblies should be cleaned after each soldering operation so that subsequent placement and soldering operations are not impaired by contamination (see 8, Cleaning Process Requirements). On assemblies using mixed component mounting technology, through-hole components should be mounted on one side of the printed board. Surface mounted components may be mounted on either or both sides of the assembly. Parts should be mounted such that part markings and reference designators are visible. Where component marking visibility and legibility is required, the contract or drawing **shall** so state. Any violation of minimum electrical clearance as a result of nonconformance to defined criteria is a defect condition.
4.15.3	**Drying/Degassing** Prior to soldering, the assembly **shall** be treated to remove detrimental moisture and other volatiles using a documented process.
4.15.4	**Holding Devices and Materials** Equipment, devices, materials, or techniques used to handle boards or retain parts and components to the printed boards through any and all stages of soldering **shall not** contaminate, damage, or degrade printed boards or components. The equipment, devices, materials or techniques should be adequate to maintain component positioning and permit solder flow through plated-through holes and/or onto terminal areas, but **shall not** constrain component leads or conductors against spring-back (e.g., by probes, tooling, etc.) during solder solidification.
4.17	**Reflow Soldering** The Manufacturer **shall** develop and maintain operating procedures describing the reflow soldering process and the proper operation of the equipment. These procedures **shall** include, as a minimum, a reproducible time/temperature envelope including the flux and solder paste application procedures and coverage, drying/degassing operation (when required), preheating operation, controlled atmosphere (if used), solder reflow operation, and a cooling operation (see 4.15.2). These steps may be part of an integral or in-line system or may be accomplished through a series of separate operations. When PCAs are required to be subjected to additional mass reflows in excess of the documented manufacturing process plan, the reason for the additional processing **shall** be documented, and notification **shall** be provided to the User within 24 hours.
4.18.1	**Exposed Surfaces** Except as noted below, exposed basis metal on end of leads or vertical edges of lands is acceptable. a. Iron based component material, e.g. Alloy 42, Kovar®, component leads, body, **shall not** be exposed. b. Exposed basis metal **shall not** prevent the formation of an acceptable solder connection. c. Exposed Organic Solderability Preservatives (OSP) **shall not** prevent the formation of an acceptable solder connection.

J-STD-001ES Table 1 Space Applications Requirements (cont.)

J001E Reference	Space Applications Requirement (as changed by this Addendum)
4.18.2	**Solder Connection Defects** The following solder joint conditions **shall** be considered defects: a. Fractured solder connections. b. Disturbed solder connections. c. Cold or rosin solder connections. d. Solder that violates minimum electrical clearance (e.g., bridges), or contacts the component body (except as noted in 7.5.7). e. Fails to comply with wetting criteria of 4.18 f. Solder bridging between joints except when path is present by design. g. Overheated solder connection. h. Blowholes and pinholes (where the bottom and all sides are not visible). i. Excessive solder (solder in the bend radius of axial leaded parts in PTHs is not cause for rejection provided the lead is properly formed, the topside bend radius is discernible, and the solder does not extend to within 1 lead diameter of the part body or end seal). j. Insufficient solder. k. Contamination (e.g., lint, flux, dirt, extraneous solder/metal).
4.18.3	**Partially Visible or Hidden Solder Connections** Partially visible or hidden solder connections are acceptable provided that the following conditions are met: a. The design does not restrict solder flow to any connection element on the solder destination side lands (e.g., PTH component) of the assembly. b. The visible portion, if any, of the connection on either side of the PTH solder connection (or the visible portion of the SMD connection) is acceptable. c. Process controls are maintained in a manner assuring repeatability of assembly techniques. d. For solder connections that do not meet any of the above conditions, NDE **shall** be used. The User **shall** approve the NDE method prior to use.
5.1.2	**Strand Damage** J-STD-001E Table 5–1 does not apply; there **shall be no** nicked, scraped or broken wire strands. See 6.1.2 of this addendum for damage requirements applicable to solid conductor wires/leads. For plated wires, a visual anomaly that does not expose basis metal is not considered to be strand damage. Smooth indentations up to 10%, e.g. tooling marks, and as allowed for intentionally flattened wires (see J-STD-001E 7.1.4), of the diameter, width, or thickness of the wire are acceptable. If the twist pattern (lay) of wire strands is disturbed, it **shall** be restored as nearly as possible to the original pattern. Wire strands **shall** not have separation exceeding 1 strand diameter or extend beyond wire insulation outside diameter. Wire strands **shall** not be altered or cut to fit terminals.
5.1.3	**Tinning of Stranded Wire** Solder used for tinning **shall** be the same alloy that will be used in subsequent soldering processes. Solder wicking **shall not** extend to a portion of the wire which is required to remain flexible. The solder **shall** wet the tinned portion of the wire and should penetrate to the inner strands of the wire. Wire strands **shall** be discernable after tinning. Solder build-up or icicles within the tinned wire area **shall** not affect subsequent assembly steps. The length of untinned strands from end of wire insulation **shall not** be greater than 1 wire diameter. Portions of stranded wire that will be soldered **shall** be tinned prior to mounting when • Wires will be formed for attachment to solder terminals. • Wires will be formed into splices (other than mesh). • Wires will be used in heat shrinkable solder device. Stranded wires **shall** not be tinned when: • Wires will be used in crimp terminations. • Wires will be used in threaded fasteners. • Wires will be used in forming mesh splices.

J-STD-001ES Table 1 Space Applications Requirements (cont.)

<table>
<tr><th>J001E Reference</th><th>Space Applications Requirement (as changed by this Addendum)</th></tr>
<tr><td>5.3.6</td><td>

Terminal Soldering Terminals mounted and soldered to the printed board **shall** meet the requirements shown in Table 5–2 of this addendum.

Table 5–2 Terminal Soldering Requirements

<table>
<tr><td>A.</td><td>Circumferential fillet and wetting – solder source side</td><td>360°</td></tr>
<tr><td>B.</td><td>Percentage of solder source side land area covered with wetted solder</td><td>75%</td></tr>
</table>

</td></tr>
<tr><td>5.5</td><td>

Soldering to Terminals A solder fillet **shall** join the wire/lead to the terminal for 100% of the lead to terminal contact area.

</td></tr>
<tr><td>6.1.1</td><td>

Lead Forming Part and component leads should be preformed to the final configuration excluding the final clinch or retention bend before assembly or installation. The lead forming process **shall not** damage lead seals, welds, or connections internal to components. Leads **shall not** be reformed except for minor adjustments to bend angles.

Leads **shall** extend at least one lead diameter or thickness but not less than 0.8 mm [0.031 in] from the body or weld before the start of the bend radius (see J-STD-001E Figure 6–1).

Note: Measurement is made from the end of the part. (The end of the part is defined to include any coating, solder seal, solder or weld bead, or any other extension.).

The lead bend radius **shall** be in accordance with Table 6–1 of this addendum.

Table 6–1 Lead Bend Radius

<table>
<tr><th>Lead Diameter</th><th>Minimum Bend Radius (R)</th></tr>
<tr><td>Less than 0.8 mm [0.031 in]</td><td>1 diameter/thickness</td></tr>
<tr><td>0.8 to 1.2 mm [0.031 to 0.047 in]</td><td>1.5 diameters/thickness</td></tr>
<tr><td>Greater than 1.2 mm [0.047 in]</td><td>2 diameters/thickness</td></tr>
</table>

</td></tr>
<tr><td>6.1.2</td><td>

Lead Deformation Limits Whether leads are formed manually or by machine or die, parts or components **shall not** be mounted if the part or component lead has any nicks, scrapes or gouges. Smooth indentations up to 10%, e.g. tooling marks, and as allowed for intentionally flattened leads (see 7.5.8), of the diameter, width, or thickness of the lead are acceptable. See 4.2.3 and 4.18.1.

</td></tr>
<tr><td>6.1.3</td><td>

Termination Requirements Component leads in supported holes may be terminated using a straight through, partially clinched, or clinched configuration. The clinch should be sufficient to provide mechanical restraint during the soldering process. The orientation of the clinch relative to any conductor is optional. DIP leads should have at least two diagonally opposing leads partially bent outward.

If a lead or wire is clinched, the lead **shall** be wetted in the clinched area. The outline of the lead should be discernible in the solder connection.

Tempered leads **shall not** be terminated with a (full) clinched configuration.

Lead protrusion **shall not** violate minimum electrical clearance requirements. Lead protrusion **shall** be in accordance with Table 6–2 of this addendum for supported holes or Table 6–3 of this addendum for unsupported holes. Presence of a lead (Table 6–2 Note 1) **shall** be verified prior to soldering.

Connector leads, relay leads, tempered leads and leads greater than1.3 mm [0.051in] diameter are exempt from the maximum length requirement provided that they do not violate minimum electrical clearance.

Table 6–2 Protrusion of Leads in Supported Holes

<table>
<tr><td>(L) min</td><td>End is discernible in solder[1]</td></tr>
<tr><td>(L) max</td><td>2.25 mm [0.0885 in]</td></tr>
</table>

Note 1. For boards greater than 2.3 mm [0.0906 in] thick, with components having pre-established lead lengths, e.g., DIPs, sockets, connectors, as a minimum need to be flush to the board surface, but may not be visible in the subsequent solder connection.

Table 6–3 Protrusion of Leads in Unsupported Holes

<table>
<tr><td>(L) min</td><td>Sufficient to clinch</td></tr>
<tr><td>(L) max[1]</td><td>No danger of shorts</td></tr>
</table>

Note 1. Lead protrusion should not exceed 2.5 mm [0.0984 in] if there is a possibility of violation of minimum electrical clearance, damage to soldered connections due to lead deflection or penetration of static protective packaging during subsequent handling or operating environments.

</td></tr>
</table>

J-STD-001ES Table 1 Space Applications Requirements (cont.)

<table>
<tr><th>J001E Reference</th><th>Space Applications Requirement (as changed by this Addendum)</th></tr>
<tr><td>6.2.2</td><td>

Through-Hole Component Lead Soldering When soldering component leads into PTH connections, the goal of the process is to accomplish 100% fill of the PTH with solder and good wetting to the lands, lead, and barrel top and bottom. The solder connection **shall** meet the requirements of Table 6–4 of this addendum, regardless of the soldering process, e.g. hand soldering, wave soldering, intrusive soldering, etc.

Table 6–4 Supported Holes with Component Leads, Minimum Acceptable Conditions[1]

<table>
<tr><td>A.</td><td>Vertical fill of solder.[2,3]</td><td>75%</td></tr>
<tr><td>B.</td><td>Circumferential wetting of lead and barrel on solder destination side.</td><td>360º</td></tr>
<tr><td>C.</td><td>Percentage of original land area covered with wetted solder on solder destination side.[3]</td><td>0</td></tr>
<tr><td>D.</td><td>Circumferential fillet and wetting of lead and barrel on solder source side.</td><td>360º</td></tr>
<tr><td>E.</td><td>Percentage of original land area covered with wetted solder on solder source side.[3]</td><td>75%</td></tr>
</table>

Note 1. Wetted solder refers to solder applied by any solder process including intrusive soldering.
Note 2. Applies to any side to which solder or solder paste was applied. The 25% unfilled height includes a sum of both source and destination side depressions.
Note 3. Provided the solder has flowed onto, and wetted to, the lead and solder land before receding.

</td></tr>
<tr><td>6.3.1</td><td>

Lead Termination Requirements for Unsupported Holes Lead protrusion for unsupported holes **shall** meet the requirements of Table 6–3 of this addendum. Solder **shall** meet the requirements of Table 6–5 of this addendum.

Table 6–5 Unsupported Holes with Component Leads, Minimum Acceptable Conditions[1]

<table>
<tr><td>Wetting of lead and land</td><td>360°</td></tr>
<tr><td>Percentage of land area covered with wetted solder[2]</td><td>75%</td></tr>
</table>

Note 1. Wetted solder refers to solder applied by the solder process.
Note 2. Solder is not required to cap or cover the hole.

</td></tr>
<tr><td>7.1</td><td>

Surface Mount Device Lead Forming Leads **shall** be formed in such a manner that the lead-to-body seal is not damaged or degraded (see J-STD-001E Figures 7–1 and 7–2). When lead forming is required during the assembly process leads **shall** be formed such that there is an available minimum lead length for contact to the solder pad as shown in Table 7–1 of this addendum.

The leads of surface mounted components **shall** be formed to their final configuration prior to soldering.

Note: Where severe loading conditions exist such as Coefficient of Thermal Expansion (CTE) mismatches or severe operational environments, extra consideration should be given to the minimum available contact length.

Table 7–1 SMT Lead Forming Minimum Lead Length

<table>
<tr><td>A.</td><td>Two lead widths for flat leads.</td></tr>
<tr><td>B.</td><td>Two lead widths for coined leads.</td></tr>
<tr><td>C.</td><td>Two lead diameters for round leads.</td></tr>
</table>

</td></tr>
<tr><td>7.1.1</td><td>

Surface Mount Device Lead Deformation There **shall be no** unintentional lead deformation beyond the limits defined in Paragraph 6.1.2.

</td></tr>
<tr><td>7.2</td><td>

Leaded Component Body Clearance The maximum clearance between the bottom of a leaded component body and the printed wiring surface should be 2.0 mm [0.0787 in]. Parts insulated from circuitry or over surfaces without exposed circuitry should be mounted flush. Uninsulated parts mounted over exposed circuitry or which are in close proximity with other conductive materials **shall** be separated by suitable insulation.

</td></tr>
<tr><td>7.5.6</td><td>

Castellated Terminations If parts with castellated terminations are chosen by design, their use **shall** be approved by the User. When used, the existing J-STD-001E Class 3 requirements apply.

</td></tr>
</table>

J-STD-001ES Table 1 Space Applications Requirements (cont.)

<table>
<tr><th>J001E Reference</th><th>Space Applications Requirement (as changed by this Addendum)</th></tr>
<tr><td>7.5.8</td><td>
Round or Flattened (Coined) Gull Wing Leads Connections formed to round or flattened (coined) leads shall meet the dimensional and fillet requirements of Table 7–8 of this addendum and J-STD-001E Figure 7–8 for each product classification.
Table 7–8 Dimensional Criteria – Round or Flattened (Coined) Gull Wing Leads
<table>
<tr><th>Feature</th><th>Dim.</th><th>Requirement</th></tr>
<tr><td>Maximum Side Overhang</td><td>A</td><td>25% (W) or 0.5 mm [0.02 in], whichever is less; Note 1</td></tr>
<tr><td>Maximum Toe Overhang</td><td>B</td><td>Note 1</td></tr>
<tr><td>Minimum End Joint Width</td><td>C</td><td>75% (W)</td></tr>
<tr><td>Minimum Side Joint Length</td><td>D</td><td>100% of available lead to land interface</td></tr>
<tr><td>Maximum Heel Fillet Height</td><td>E</td><td>Note 4</td></tr>
<tr><td>Minimum Heel Fillet Height</td><td>F</td><td>(G) +(T) Note 5</td></tr>
<tr><td>Solder Thickness</td><td>G</td><td>Note 3</td></tr>
<tr><td>Formed Foot Length</td><td>L</td><td>Note 2</td></tr>
<tr><td>Minimum Side Joint Height</td><td>Q</td><td>(G) + 50% (T)</td></tr>
<tr><td>Thickness of Lead at Joint Side</td><td>T</td><td>Note 2</td></tr>
<tr><td>Flattened Lead Width or Diameter of Round Lead</td><td>W</td><td>Note 2</td></tr>
</table>
Note 1. Does not violate minimum electrical clearance.
Note 2. Unspecified parameter or variable in size as determined by design.
Note 3. Wetting is evident.
Note 4. Solder fillet may extend through the top bend. Solder does not touch package body or end seal. Solder should not extend under the body of surface mount components whose leads are made of Alloy 42 or similar metals.
Note 5. In the case of a toe-down lead configuration, the minimum heel fillet height (F) extends at least to the mid-point of the outside lead bend.
</td></tr>
<tr><td>7.5.14</td><td>
Surface Mount Area Array Packages The area array criteria defined herein assumes an inspection process is established to determine compliance for either X-Ray or normal visual inspection processes. To a limited extent, this may involve visual assessment, but evaluation of X-Ray images shall be used to allow assessment of characteristics that cannot be accomplished by normal visual means.
Visual inspection requirements:

When visual inspection is the method used to verify product acceptance the magnification levels of J-STD-001E Tables 11–1 and 11–2 apply.
The solder terminations on the outside row (perimeter) of the area array component shall be visually inspected.
The area array component needs to align in both X & Y directions with the corner markers on the PCB (if present).
Absence of leads, e.g. solder ball or columns, are defects unless specified by design.

Process development and control is essential for continued success of assembly methods and implementation of materials.
Area array process guidance is provided in IPC-7095, which contains recommendations developed from extensive discussion of process development issues.
Note: X-ray equipment not intended for electronic assemblies or not properly set up can damage sensitive components.
Surface mount area array packages shall meet the dimensional and solder fillet requirements of J-STD-001E Table 7–14 for components with collapsing balls, J-STD-001E Table 7–15 for components with noncollapsing balls, and J-STD-001E Table 7–16 for column grid arrays.
</td></tr>
</table>

J-STD-001ES Table 1 Space Applications Requirements (cont.)

J001E Reference	Space Applications Requirement (as changed by this Addendum)
7.5.15	**Bottom Termination Components (BTC)** These criteria are also applicable to Small Outline Integrated Circuit (No Leads) (SOICNL). Criteria for nonvisible part of thermal plane solder connections (including voids) are not described in this document and shall be established by agreement between the Manufacturer and the User. The thermal transfer plane acceptance criteria are design and process related. Issues to consider include but are not limited to component manufacturer's application notes, solder coverage, voids, solder height, maximum junction temperature, etc. When soldering these types of components voiding in the thermal plane is common. Solder, when required, **shall** meet documented requirements. Connections formed to components having no significant external lead form **shall** meet the dimensional and solder fillet requirements of Table 7–17 of this addendum and J-STD-001E Figure 7–15. There are some package configurations that have no toe exposed or do not have a continuous solderable surface on the exposed toe on the exterior of the package and a toe fillet will not form. Bottom Termination Component (BTC) process guidance is provided in IPC-7093, which contains recommendations developed from extensive discussion of BTC process development issues. Process development and control is essential for continued success of assembly methods and implementation of materials. Evaluation of X-Ray images **shall** be used to allow assessment of characteristics that cannot be accomplished by normal visual means (e.g., if a criterion for voids is established).

Table 7–17 Dimensional Criteria – BTC

Feature	Dim.	Requirement
Maximum Side Overhang	A	25% (W), Note 1
Toe Overhang (outside edge of component termination)	B	Not Permitted'
Minimum End Joint Width	C	75% (W)
Minimum Side Joint Length	D	Note 4
Minimum Toe (End) Fillet Height	F	Notes 2, 5
Solder Fillet Thickness	G	Note 3
Termination Height	H	Note 5
Solder Coverage of Thermal Land		Note 4
Land Width	P	Note 2
Termination Width	W	Note 2
Thermal Plane Void Criteria		Note 6

Note 1. Does not violate minimum electrical clearance.
Note 2. Unspecified parameter or variable in size as determined by design.
Note 3. Wetting is evident.
Note 4. Not a visually inspectable attribute. See 4.18.3.
Note 5. (H) = height of solderable surface of lead, if present. Some package configurations do not have a continuous solderable surface on the sides and do not require a toe (end) fillet.
Note 6. Required when criteria are established between the Manufacturer and the User

J-STD-001ES Table 1 Space Applications Requirements (cont.)

J001E Reference	Space Applications Requirement (as changed by this Addendum)
7.5.16	**Components with Bottom Thermal Plane Terminations (D-Pak)** Criteria for nonvisible parts of thermal plane solder connections are not described in this document and will need to be established by agreement between the Manufacturer and the User. The thermal transfer plane acceptance criteria are design and process related. Issues to consider include but are not limited to component manufacturer's application notes, solder coverage, voids, solder height, etc. Solder, when required, **shall** meet documented requirements. When soldering these types of components voiding in the thermal plane is common. Evaluation of X-Ray images **shall** be used to allow assessment of characteristics that cannot be accomplished by normal visual means (e.g., if a criterion for a void is established). **Note:** The criteria for leads other than the thermal plane termination are provided in the criteria for the type of lead termination used. Connections formed to components with bottom thermal plane terminations shall meet the dimensional and solder fillet requirements of Table 7–18 of this addendum.

Table 7–18 Dimensional Criteria – Bottom Thermal Plane Terminations

Feature (all connections except thermal plane)	Dim.	
Maximum Side Overhang	A	The mounting and solder requirements for SMT terminations **shall** meet the criteria for the type of lead termination being used.
Toe Overhang	B	
Minimum End Joint Width	C	
Minimum Side Joint Length	D	
Maximum Heel Fillet Height	E	
Minimum Heel Fillet Height	F	
Solder Fillet Thickness	G	
Lead Thickness	T	
Feature (only for the thermal plane connection)		
Thermal Plane Side Overhang (J-STD-001E Figure 7–16)		Not greater than 25% of termination width.
Thermal Plane End Overhang		No overhang.
Thermal Plane End Joint Width		100% wetting to land in the end-joint contact area.

J001E Reference	Space Applications Requirement (as changed by this Addendum)
7.5.17	**Flatten Post Connections/Square Solder Land, Round Flatten Post** If parts with flattened post terminations are chosen by design, their use, including acceptance criteria, **shall** be approved by the User.
8.3	**Post Solder Cleanliness** Inspection is used to assess the presence of visible foreign particulate matter as required in 8.3.1, or flux and other ionic or organic residues as required in 8.3.2 (see 11.2.2). Surfaces cleaned **shall** be inspected between 4X and 10X magnification and **shall** be free of visual evidence of residue or contaminants.
8.3.1	**Particulate Matter** Assemblies **shall** be free of dirt, lint, solder splash, dross, wire clippings, solder balls or other metal particles, etc. Solder balls are allowed if proven secured (i.e., will not come loose during transportation, storage, or operation of the system) with a documented specialized process. The specialized process and acceptance criteria **shall** be approved by the User prior to use. The approved process **shall** be applied to 100% of all solder balls. Data generated by the approved process **shall** be maintained and available for review. Any violation of minimum electrical clearance **shall** be a defect, see 4.9.
8.3.2	**Flux Residues and Other Ionic or Organic Contaminants** Unless specified otherwise on engineering documentation approved by the User, cleanliness designator C-22 as described in the following paragraphs and the visual requirements for cleanliness (per 8.3) **shall** apply to all assemblies.

J-STD-001ES Table 1 Space Applications Requirements (cont.)

J001E Reference	Space Applications Requirement (as changed by this Addendum)
9.1.1	**Blistering/Delamination** There **shall** be no blistering or delamination between any of the laminate layers, or between the laminate and the metallization. **Note:** Measling is NOT the same as blistering or delamination. See IPC-T-50 and IPC-A-610 for clarification.
9.1.2	**Weave Exposure/Cut Fibers** There **shall** be no non-wetted exposed glass fibers. There **shall** be no surface damage that cuts into laminate fibers. Exception: Exposed fibers may extend onto the top and bottom surfaces of the printed board a maximum of 0.6mm [0.0236 in] around the perimeter of the printed board or around unsupported holes without lands.
9.1.4	**Land/Conductor Separation** The outer, lower edge of land areas **shall not** be lifted or separated more than the thickness (height) of the land. Land areas **shall not** be lifted when there is an unfilled via or via with no lead in the land. There **shall** be no separation of circuit conductors from the base laminate.
9.1.10	**Measles** Measles **shall not** bridge non-common conductors.
10	**Coating, Encapsulation and Staking (Adhesive)** a. A mix record shall be created for each mixed batch of multi-part polymers used for conformal coating, encapsulating, or staking. At a minimum, this record **shall** include the date mixed, manufacturer's part number and date/lot code, shelf-life expiration date (of all parts of the mix), and the mix ratio for all constituents used. b. For one-part polymers, the manufacturer's part number and lot/date code, and shelf life expiration date **shall** be documented. c. Materials **shall** be cured in accordance a documented cure schedule and within the thermal limitations of the hardware. Objective evidence of full cure for each batch of material **shall** be documented. A witness sample may be used for this verification. d. When coating, encapsulation, or staking materials are applied to through-hole glass, ceramic body, or hermetic components, the components **shall** be protected to prevent cracking, unless the material has been selected so as not to damage the components/assembly in its service environment. e. Equipment used for processing silicone material **shall not** be used for processing other material. f. Prior to conformal coating, staking or encapsulating, the assembly and any fillers used (e.g., thickening agents, thermal property enhancers, etc) **shall** be treated to remove detrimental moisture and other volatiles. g. When fluorescent conformal coating materials are used, coverage and location **shall** be determined by UV-light examination. h. Areas to be coated, encapsulated, and/or staked **shall** be cleaned prior to material application. i. Non-porous containers and mixing tools **shall** be used. Containers and mixing tools **shall** be selected such that their use in combination cannot introduce contamination into the mix, e.g., a metal stirrer can scrape shavings from a plastic container.
10.1.4	**Rework of Conformal Coating** Procedures that describe the removal and replacement of conformal coating **shall** be documented and available for review. Chemical stripping processes **shall** be approved by the User prior to use.
10.3	**Staking (Adhesive)** The staking criteria below **shall** be used when criteria are not provided by the drawing. **a. Documentation** Components to be staked **shall** be identified on the assembly drawing(s)/ documentation. Some component packages should always be staked (e.g., axial leaded solid-slug tantalum capacitors). Components identified as required to be staked on the assembly drawing(s)/ documentation **shall** be staked. **b. Placement** Staking materials **shall not** contact component lead seals unless the material has been selected so as not to damage the components/assembly in its service environment. **c. Unsleeved axial leaded components mounted horizontally** – Staking material **shall** be applied to both sides of the component. The length of the fillets of the staking material **shall** be minimum 50% to a maximum 100% of the length of the component. The minimum fillet height **shall** be 25% of the height of the component. The maximum fillet height **shall** be that the top of the component is visible for the entire length of the component. See Figure 10–1 of this addendum. **d. Unsleeved axial leaded components mounted vertically** – A minimum of three beads of staking material **shall** be placed approximately evenly around the periphery of the component. For each bead, the staking material **shall** contact a minimum-25% to maximum-100% of the height of the component body. Slight flow of staking material under the component body is acceptable provided it does not violate 10.3b.

J-STD-001ES Table 1 Space Applications Requirements (cont.)

J001E Reference	Space Applications Requirement (as changed by this Addendum)
	e. Sleeved axial leaded components This clause does not apply to sleeved glass bodied axial leaded components (see 10.3f). In addition to the requirement of 10.3 c, staking material **shall** be in contact with both end-faces of the component and the surface it is being staked to. The minimum fillet height **shall** be at least 25% of the height of the component. The maximum fillet height **shall** be no greater than 50% of the height of the component, and **shall not** violate 10.3.b. See Figure 10–2 of this addendum. **f. Glass Bodied Components** Sleeved glass bodied components **shall** be free from staking material on any exposed glass surface, such as the component end face. Staking material **shall** be applied to both sides of the component. Staking material fillet **shall** extend between 50% and 100% of the component length. Minimum fillet height **shall** be 25% of the component height. Maximum fillet height **shall** allow the top of the component to be visible for the entire length of the component body. **g. Radial leaded components – longest dimension is height (e.g., CKR capacitors, Single In-Line (SIP) resistor net-works)** Individual components **shall** be staked in accordance with Figure 10–3 of this addendum. The staking material **shall** be applied to a minimum height of 25% to a maximum of 100% of the component body height. Closely spaced arrays consisting of up to four components **shall** be staked in accordance with Figure 10–4 of this addendum. Fillet height requirements for the two outer end-faces **shall** be the same as for an individual component. In addition, the top inner surfaces **shall** be bonded to each other for at least 50% of the components' width. Closely spaced arrays consisting of more than four components **shall** be staked in accordance with Figure 10–5 of this addendum. Staking **shall** be applied in the same manner as arrays up to four components, with the additional requirement that every other internal component **shall** have their sides staked to the board surface. **h. Radial leaded components – longest dimension is diameter or length (e.g., TO5 semiconductors, etc.).** Cylindrical components **shall** be staked in accordance with Figure 10–6 of this addendum. At least three beads of staking material **shall** be placed approximately evenly around the periphery of the component. For each bead, the staking material **shall** contact a minimum-25% to maximum-100% of the height of the component body. Slight flow of staking material under the component body is acceptable provided it does not violate 10.3b. Rectangular components **shall** be staked in accordance with Figure 10–7 of this addendum. A bead of staking material **shall** be placed at each corner of the component. For each bead, the staking material **shall** contact a minimum-25% to maximum-100% of the height of the component body. Slight flow of staking material under the component body is acceptable provided it does not violate 10.3b. **i. Fasteners** Fasteners identified on the drawing to be staked **shall** be staked either: • At two places spaced approximately opposite of each other. Each bead of staking material **shall** cover at least 25% of the perimeter of the fastener in accordance with Figure 10–8 of this addendum. • One bead of staking material that covers at least 50% of the perimeter of the fastener in accordance with Figure 10–9 of this addendum.
11.2.2	**Visual Inspection** After the soldering and cleaning process is complete, all assemblies **shall** be evaluated by 100% visual or nondestructive inspection (see 1.11) except for solder connections as specified in 4.18.3, 7.5.14, 7.5.15 and 7.5.16. When assemblies are to be conformally coated and/or staked or encapsulated, the coating, encapsulation, and/or staking **shall** be evaluated by 100% visual inspection. Inspection of conformal coating, staking or encapsulation **shall** be performed after and not combined with, soldering and cleaning process inspections.
11.2.3	**Sampling Inspection** Sampling inspection **shall** be prohibited unless approved by the User prior to use.
12.2	**Repair** A hardware defect **shall not** be repaired until the discrepancy has been documented and only after authorization from the User for each incident. The repair method **shall** be determined by agreement between the Manufacturer and the User.

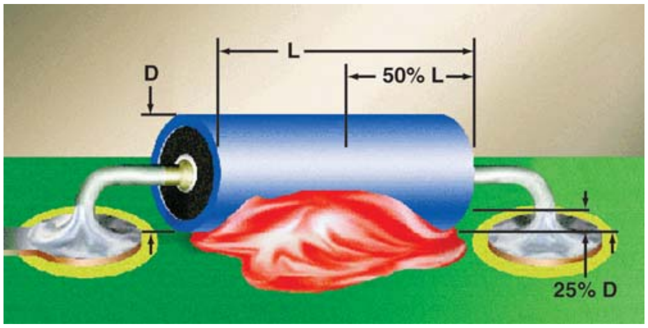


Figure 10–1

Acceptable

- Fillet Length: 50%L, to 100%L.
- Fillet Height: 25%D to 100%D. Top of component is visible for its entire length.

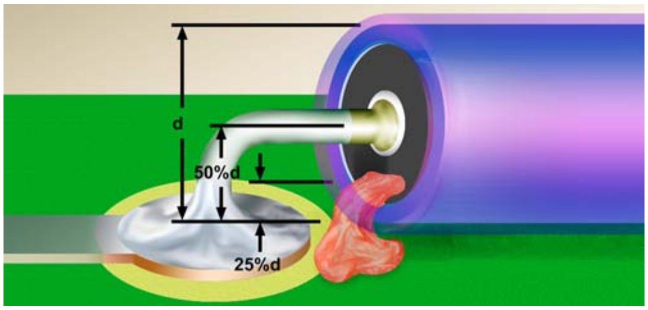


Figure 10–2

Acceptable

- Staking is in contact with both end-faces of component (see 10.3.e).
- Fillet Height: 25%D to 50%D and does not contact lead seals or solder termination (see 10.3.b).

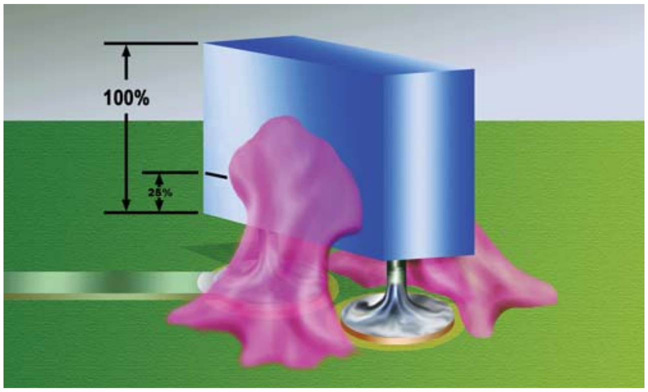


Figure 10–3

Acceptable

- Fillet Height 25%H to 100%H.

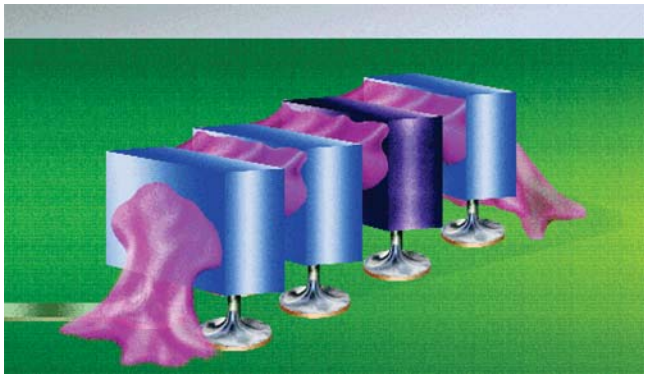


Figure 10–4

Acceptable

- Two outside ends – fillet height: 25%H to 100%H.
- Inner surfaces – fillet is in contact with both surfaces for at least 50% of component width.

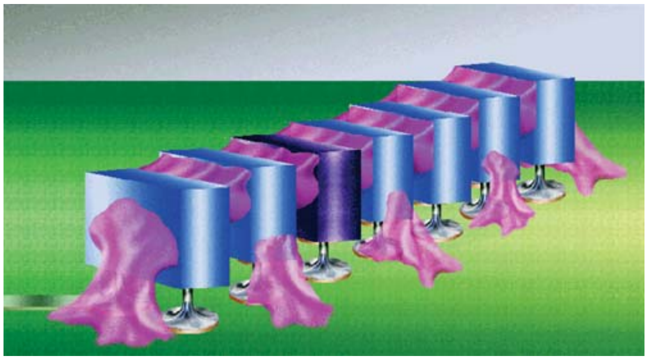


Figure 10–5

Acceptable

- Two outside ends – fillet height: 25%H to 100%H.
- Inner surfaces – fillet is in contact with both surfaces for at least 50% of component width.
- Side of every other internal component is staked to board surface.

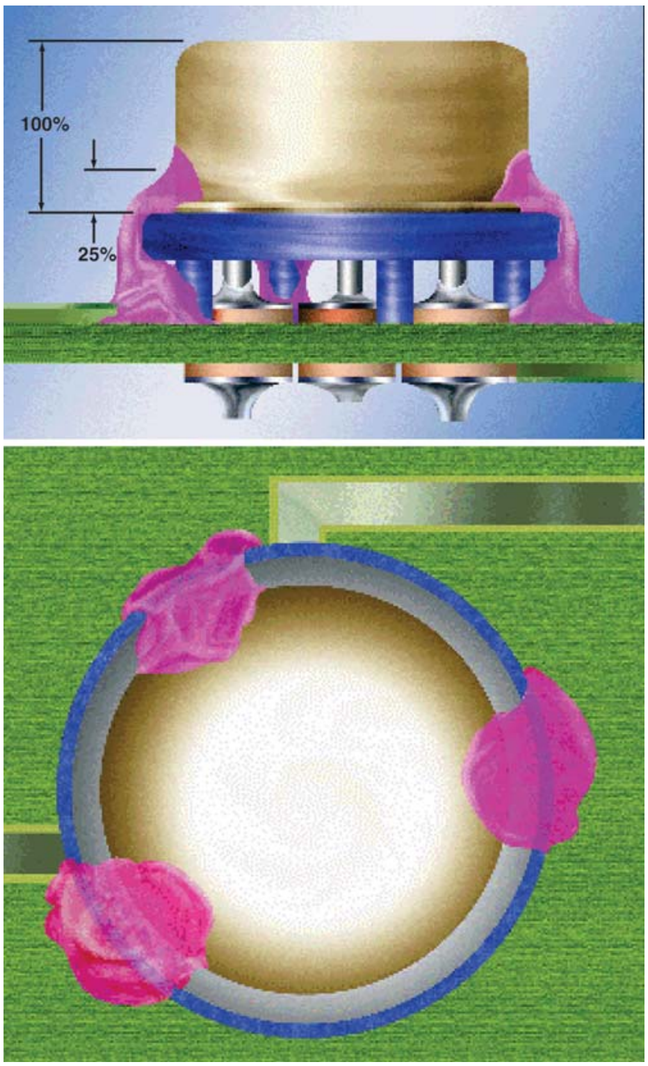


Figure 10–6

Acceptable

- At least 3 beads spaced approximately evenly around periphery of component.
- Each bead fillet height 25%H to 100%H.
- Slight flow underneath component, but bead(s) do not contact lead seals (see 10.3.b).

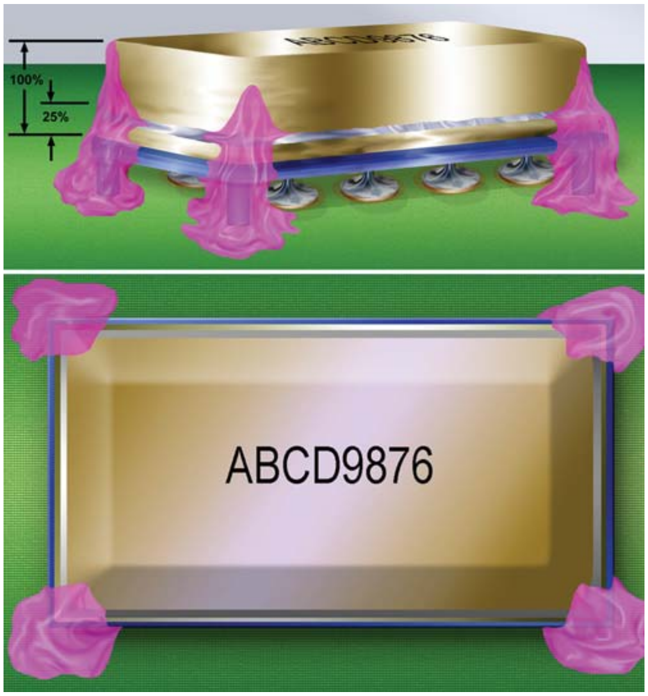


Figure 10–7

Acceptable

- One bead at each corner of the component.
- Each bead fillet height 25%H to 100%H.
- Slight flow underneath component, but bead(s) do not contact lead seals or solder termination (see 10.3.b).

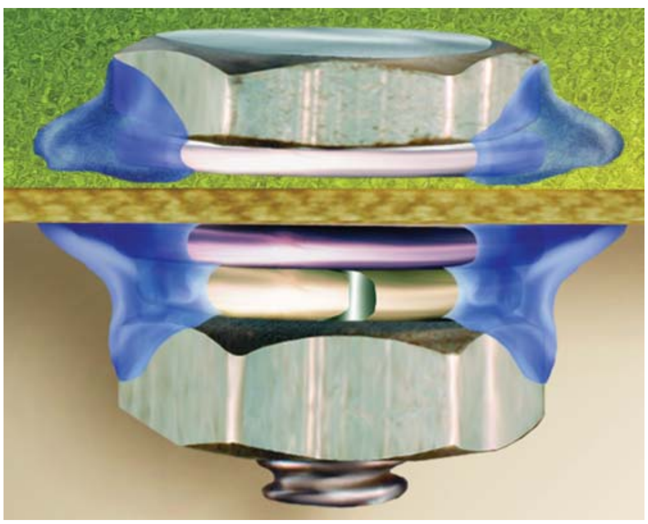


Figure 10–8

Acceptable

- Two beads of staking material placed approximately opposite of each other.
- Each bead of staking material is at least 25% of the perimeter of the fastener.

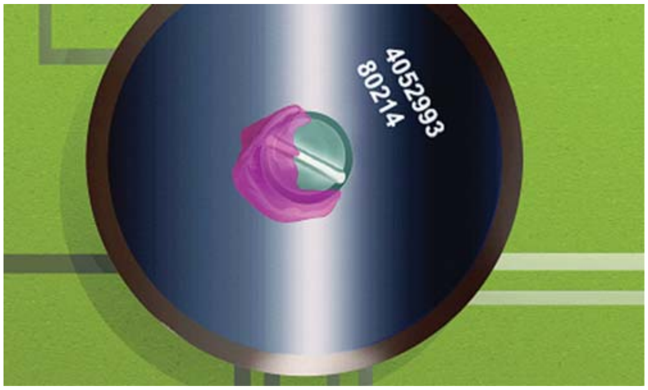


Figure 10–9

Acceptable

- One bead of staking material that covers at least 50% of the perimeter of the fastener.

Standard Improvement Form

IPC J-STD-001ES

The purpose of this form is to provide the Technical Committee of IPC with input from the industry regarding usage of the subject standard.

Individuals or companies are invited to submit comments to IPC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

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1. I recommend changes to the following:

___ Requirement, paragraph number __________

___ Test Method number __________, paragraph number __________

The referenced paragraph number has proven to be:

___ Unclear ___ Too Rigid ___ In Error

___ Other ______________________________

2. Recommendations for correction:

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3. Other suggestions for document improvement:

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ISBN #1-580986-82-X